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| 09/750,200 | 12/27/2000 | Chih-Jen Lin | 42390.P9480 | 7005 |

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| EXAMINER | |
|---|---|
| DINH, PAUL | |
| **ART UNIT** | **PAPER NUMBER** |
| 2825 | |

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/750,200 | LIN ET AL. | |
| | Examiner | Art Unit | |
| | Paul Dinh | 2825 | |

*-- Th MAILING DATE of this communication app ars on the cov r sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11/28/03*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This final office action is a response to the amendment + remarks filed on 11/28/03. The amendment does not overcome prior art and the remarks are not persuasive. Therefore,

The previous rejections based on Koenemann and Motika are retained; and

New grounds of rejections have been cited in this office action in view of the amendment; see the following details.

### Specification

Page 5, lines 14-15, are objected to because:

"WG 112b provides an input to a scan chain 112b, WG 112c provides an input to a scan chain **112c**" should be changed to "WG 112b provides an input to a scan chain [112b] 104b, WG 112c provides an input to a scan chain [112c] 104c ".

### Claims objections

The dependencies of claim 1, in general, are objected to because they have not been checked to the extent necessary to determine the presence of all possible basic errors, lack of clarity and antecedent basis problems after claim 1 have been amended by the applicant after the first office action. Applicant's cooperation is requested in correcting any possible errors, lack of clarity and antecedent basis problems of which applicant may become aware in the claims. Here are some examples:

Claims 2-3, 5-6, 8, 13 are objected to because:

(Claim 2) "the switch" lacks antecedent basis. All "switch" should be changed to "multiplexer" for consistency.

(Claim 2) "the corresponding data field" lacks antecedent basis because " a corresponding data field" has been deleted from claim 1.

(Claim 3) "the memory" lacks antecedent basis because "a memory" has been deleted from claim 1.

(Claim 5) "the memory", "the corresponding test data bit" and "said test data bit stream" lack antecedent basis due to amendment in claim 1.

(Claim 6) "the data set" and "the memory" lack antecedent basis due to amendment in claim 1.

(Claim 8) "wherein each data field", "the data set" and "the memory" lack antecedent basis due to amendment in claim 1.

(Claim 13) in the previous office action, "Claims 2 and 13 are objected to because "a switch" should be changed to - - a [switch] multiplexer - - for clarification/accuracy and less confusing; see multiplexer symbol 152 in fig 2". The applicant changes "switch" to multiplexer in claim 2 (see detailed above claim 2 objection) and fails to amend claim 13. This is a second reminder; the applicant is advised to amended claim 13 to overcome the objection.

***Claim Rejections - 35 USC § 102***

*The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:*

*A person shall be entitled to a patent unless –*

*(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

1. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Koenemann Et al (USP 5612963) who discloses a circuit/method comprising:

(Claim 1) a pseudo-random pattern generator coupled to provide pseudo-random pattern *(element PRPG 10 in fig 4, col 1 lines 64-65, element LFSR 10 in fig 2-3 generates pseudo-random pattern)*;

at least one on-die *(see on-chip in abstract/background/summary/col 4-5, 8 for all on-die/on the die/IC die limitations)* weight generator circuit *(weight generator circuit is elements 11-15 in fig 2, elements 16, 20, 20' in fig 4 (weighting circuitry 20' comprise bank of individual weighting generator circuits 20))* coupled to receive the pseudo-random pattern and to provide pseudo random weighted input bits (outputs of 20, 20') to at least one scan chain *(element 19A, 19B, 19N, SCAN CHANNEL 1, 2, ...N)*;

circuitry (30 of fig 4) coupled to provide at least one random weight determining signal *(signal from element 30 in fig 4)* to the weight generator circuit, each random weight determining signal having a weighted valued to determine one of the pseudo random weighted input bits; and

a data download circuit (fig 2-4 function as data download circuit, elements 31-33 and address signals, controls signals that coupled to elements 31-33 are also data down load circuit) to download each random weight determining signal to the weight generator circuit in synchronization with the weight generator circuit providing the pseudo random weighted input bits to a scan chain *(element 19A, 19B, 19N, SCAN CHANNEL 1, 2, ...N).*

(Claim 10) providing a weighted test data bit stream (output of elements 20, 20' in fig 4) from a weight generating unit *(weight generator unit is elements 11-15 in fig 2, elements 16, 20, 20' in fig 4 (weighting circuitry 20' comprise bank of individual weighting generator unit 20) to a scan chain (element 19A, 19B, 19N, SCAN CHANNEL 1, 2, ...N)* disposed on an integrated circuit die (*see on-chip in*

*abstract/background/ summary/col 4-5, 8 for all on-die/on the die/IC die limitations)* wherein the weight of a bit of the bit stream depends upon a corresponding data field (data field from element 30) downloaded to the weight generating unit of a data set (data set in memory 31 of fig 4);

storing at least one data set in a memory unit (RAM 31 of fig 4); and

downloading to the weight generating unit (20, 20') the corresponding data field from the memory (RAM 31) in synchronization with the bit of the bit stream (output of elements 20, 20' in fig 4).

(Claim 15) an at least one weight generator circuit *(weight generator unit is elements 11-15 in fig 2, elements 16, 20, 20' in fig 4 (weighting circuitry 20' comprise bank of individual weighting generator circuit 20) to a scan chain (element 19A, 19B, 19N, SCAN CHANNEL 1, 2, ... N)*, each said weight generator circuit to provide a distinct test data bit stream to a distinct integrated circuit test scan chain *(element 19A, 19B, 19N, SCAN CHANNEL 1, 2, ... N)*,

wherein each said weight generator circuit is to determine a bit of a provided test data bit stream weight depending upon a corresponding stored control signal (stored control signal in RAM 30 of fig 4) provided to the weight generator circuit from a control signal generating unit (elements 32-33 and control circuits that generate control/read/write/address signals coupled to 32-33) disposed on the die of the integrated circuit *(see on-chip in abstract/background/ summary/col 4-5, 8 for all on-die/on the die/IC die limitations)*.

(Claims 2, 13) the weight generator circuit includes a multiplexer (14 of fig 2) to generate each weighted test data bit, the [switch] multiplexer having an input of a plural number of differently weight bit stream and a control signal of [the] a corresponding data field (1/2, ¼, 1/8, 1/16, S1-2)

(Claims 3-4, 11-12) [the] memory/data download circuit/weight generating unit/circuit is/are on-die/disposed on IC die (see on-chip in abstract/background/summary/col 4-5, 8 and fig 2-4)

(Claim 5) [the] a memory (31 of fig 4) further is to store an least on other data set; and the data download circuit is to download each data filed of each of the data set in synchronization with the weight generator circuit providing [the] corresponding test data bit to each [said] test data bit stream for each data set (fig 2-4)

(Claim 6) the data down load circuit includes a control circuit (32-33 and control circuit that generate control/read/write/address signals coupled to 32-33) to read each data field of the data set from [the] a memory (31) to a buffer system (32) and the buffer system to output each data field from the from the data down load circuit to the weight generator circuit.

(Claims 7, 9) the buffer (32) is to output the first the first data to the weight generator circuit in response to a signal from the control circuit (32-33 and control circuit that generate control/read/ write/address signals coupled to 32-33)

(Claims 8, 14) [wherein each] data field (in fig 2-4) consists of a first range of bit and the data download includes a control circuit to read a data of the data set from the memory at a second ranged of bits at a second time period to a buffer circuit, and the buffer circuit to output each data field from the data down load circuit to the weight generator circuit at a second time periods (fig 2-4)

(Claim 16) the control signal-generating unit includes both a memory unit (31) and a control circuit (32-33 and control circuit that generate control/read/ write/address signals coupled to 32-33) to download each of the stored control signals from the memory unit to the weight generator circuit in synchronization with the weight generator circuit-determining bit

(Claim 17) the memory unit (31) is a memory unit of the IC.

2. Claims 1-5, 10-13, 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Motika et al (USP 5983380) who discloses a circuit/method comprising:

(Claim 1) a pseudo-random pattern generator (element 12 in fig 2-6) coupled to provide pseudo-random pattern (col 5 lines 43-44*)*;

at least one on-die (see on-chip/IC chip/embedded in col 6 and fig 5-6 for all on-die/on the die/IC die limitations*)* weight generator circuit *(elements 118, 120, 122, 124, 126 in fig 2-6)* coupled to receive the pseudo-random pattern and to provide pseudo random weighted input bits to at least one scan chain *(elements 128, 130, 132, 134, 136 in fig 2-6)*;

circuitry (152 in fig 5-6) coupled to provide at least one random weight determining signal to the weight generator circuit, each random weight determining signal having a weighted valued to determine one of the pseudo random weighted input bits; and

a data download circuit (fig 2-6 function as data download circuit, element 154 and address signals, controls signals that coupled to element 154 are also data down load circuit) to download each random weight determining signal to the weight generator circuit in synchronization with the weight generator circuit providing the pseudo random weighted input bits to a scan chain *(elements 128, 130, 132, 134, 136 in fig 2-6)*.

(Claim 10) providing a weighted test data bit stream (output of *elements 118, 120, 122, 124, 126 in fig 2-6)* from a weight generating unit (*elements 118, 120, 122, 124, 126 in fig 2-6)* disposed on an

integrated circuit die (see on-chip/IC chip/embedded in col 6 and fig 5-6 for all on-die/on the die/IC die limitations)

wherein the weight of a bit of the bit stream depends upon a corresponding data field (data field from element 152 in fig 5-6) downloaded to the weight generating unit of a data set (data set in element 152);

storing at least one data set in a memory unit (element 152); and

downloading to the weight generating unit the corresponding data field from the memory (152) in synchronization with the bit of the bit stream (output of *elements 118, 120, 122, 124, 126 in fig 2-6*).

(Claim 15) an at least one weight generator circuit *(elements 118, 120, 122, 124, 126 in fig 2-6) to a scan chain (element)*, each said weight generator circuit to provide a distinct test data bit stream to a distinct integrated circuit test scan chain *(elements 128, 130, 132, 134, 136 in fig 2-6)*,

wherein each said weight generator circuit is to determine a bit of a provided test data bit stream weight depending upon a corresponding stored control signal (stored control signal in element 152 fig 5-6) provided to the weight generator circuit from a control signal generating unit (element 154) disposed on the die of the integrated circuit .

(Claims 2, 13) the weight generator circuit includes a multiplexer (multiplexer in fig 2-6) to generate each weighted test data bit, the multiplexer having an input of a plural number of differently weight bit stream and a control signal of the corresponding data field (152, 154)

(Claims 3-4, 11-12) the memory/data download circuit/weight generating unit/circuit is/are on-die/disposed on IC die (see on-chip/IC chip/embedded in col 6 and fig 2-6)

(Claim 5) [the] a memory (152) further is to stored at least on other data set; and the data download circuit is to download each data filed of each of the data set in synchronization with the weight generator circuit providing the corresponding test data bit to each said test data bit stream for each data set (fig 2-6)

(Claim 16) the control signal generating unit includes both a memory unit and a control circuit (fig 152, 154 in fig 5-6) to down load each of the stored control signal from the memory unit to the weight generator circuit in synchronization with the weight generator circuit determining bit.

(Claim 17) the memory unit (152) is a memory unit of the IC.

**Response to Applicant Remarks**

Note that independence claims 10, 15 have been rejected in the previous office action as a similarity to original independent claim 1, now claims 10, 15 are rejected as stand-alones as claim 1 has been amended and claims 10, 15 have not been amended.

Both Koenemann and Motika clearly teach and anticipate claims 1-17 as detailed above, this office action is final.

*Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-282-1907. The fax number for the organization handling this application is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Paul Dinh
Patent Examiner

MATTHEW SMITH
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